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(54) Method and circuit for PWM mode driving a bridge and disk guide using the same

(57) The present circuit for driving by the PWM procedure a bridge circuit BR of the type having a signal input I1,I2 and a signal output O1-O2 and at least two conduction control signals C1 and C2 comprises a first virtually-square-wave generator CO1 having an output coupled to one of the two control inputs and a second virtually-square-wave generator CO2 having an output coupled to the other of the two control inputs. In this manner, the bridge being driven by two square waves, the null value of the current at the output O1-O2 no longer constitutes an intrinsic discontinuity and any value, even around zero, is controllable with relative ease.

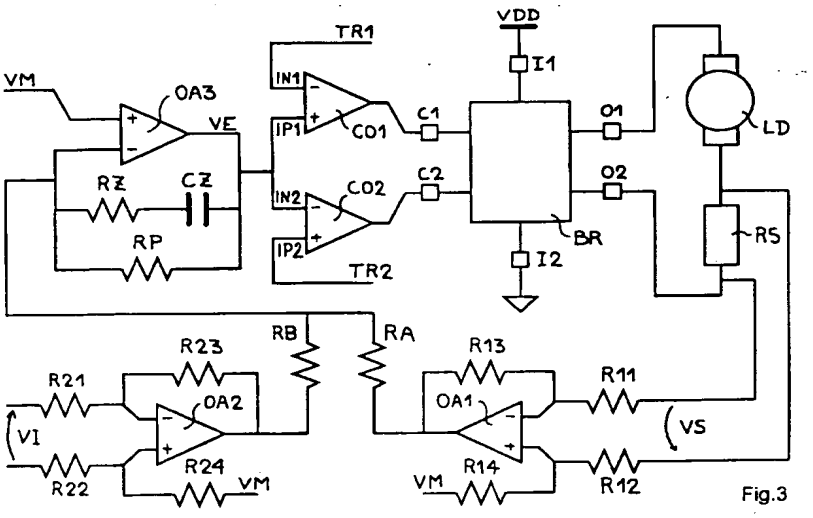

Fig.3

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Description

The present invention relates to a method of driving by the PWM procedure a bridge in accordance with the preamble of claim 1 and to a corresponding circuit in accordance with the preamble of claim 7.

Driving of loads by the Pulse Width Modulation (PWM) procedure through output stages consisting of bridge circuits is a fairly widespread practice in various electrical systems and in particular for direct current spindle motors and direct current voice coil motors. It is often useful to be able to control not only the intensity but also the direction of the current supplied to the load by the bridge circuit.

A complete collection of articles on this subject can be found in the catalog of SGS-THOMSON MICROELECTRONICS, "Designers' Guide to Power Products", June 1992 version, in the chapter entitled "DC and Brushless Motors".

The simplified diagram of a bridge circuit is shown in the annexed FIG. 1. It has two terminals I1 and I2 for a signal input, two terminals 01 and 02 for a signal output and two terminals C1 and C2 for control inputs and comprises four n-channel MOS transistors T1, T2, T3 and T4 whose main conduction paths, i.e. drain-source, constitute the branches of the bridge circuit. The control terminal of the transistor T1 is connected directly to the terminal C1, the control terminal of the transistor T2 is connected to the terminal C1 through an inverter P1, the control terminal of the transistor T3 is connected directly to the terminal C2, the control terminal of the transistor T4 is connected to the terminal C2 through an inverter P2, and between the terminals 01 and 02 is placed a load LD represented by a motor symbol but not part of the bridge circuit.

Normally to the terminal I1 is coupled a power potential reference VDD and to the terminal I2 is coupled a ground potential reference GND as shown in the annexed FIG. 2.

If the potential at the terminal C1 is high the transistor T1 is on and the transistor T2 is off. If the potential at the terminal C1 is low the transistor T1 is off and the transistor T2 is on. All this applies similarly for the terminal C2 and the transistors T3 and T4.

By applying appropriately conduction control signals to the terminals C1 and C2 there can be obtained at the output 01-02 a voltage signal having a virtually square wave form with duty cycle such that the average current flowing in the load connected to the output 01-02 of the bridge circuit assumes the desired value.

A simple and known way to drive the control inputs C1 and C2 of the bridge circuit is to send to one of the inputs, e.g. C1, a first voltage conduction control signal having a constant value and to the other input, e.g. C2, a second voltage conduction control signal consisting of a virtually square wave. By controlling the duty cycle of this second signal one controls the duty cycle of the output 01-02 and consequently the intensity of the average current in the load LD. When it is desired to obtain an average current of the same intensity but opposite direction it suffices to send the first signal to the input C2 and the second signal to the input C1.

In the annexed FIG. 2, corresponding to the figure shown on page 231 of the above mentioned catalog, is shown a bridge circuit BR like the one shown in FIG. 1 and having input terminal I1 connected to the reference VDD and input terminal I2 coupled to the reference GND in combination with a driving circuit comprising an oscillator OS0 designed to generate at one of its outputs square waves with fixed frequency and duty cycle, a resistor RS (for detection only of the current module) connected between the terminal I2 and the reference GND, a comparator CO0 having a non-inverting input connected to the resistor RS and an inverting input receiving a reference signal VR corresponding to the desired current at the output 01-02, a flip-flop FF of the SR type and having set terminal S connected to the output of the oscillator OS0 and reset terminal R connected to an output of the comparator CO0, and two AND logical gates G1 and G2 having first inputs connected together to a state output Q of the flip-flop FF and second inputs receiving respectively two logical signals L1 and L2, one inverted with respect to the other.

The circuit of FIG. 2 operates in accordance with the principle just described. Indeed, one of the signals L1 and L2 will necessarily have a low logical value and thus the output of the AND logical gate to which it is connected will have a low logical value regardless of the logical value of the output Q. At operating condition there will be present at the output Q a square wave with constant frequency and constant average duty cycle linked to the value of the signal VR. This is constant frequency operation. A similar effect would be obtained using in the circuit of FIG. 2, in place of the oscillator OS0 and the flip-flop FF, a monostable circuit started by the output of the comparator CO0. At operating condition however at the output of the monostable would be obtained a square wave with constant average frequency and constant average duty cycle. This is constant off time (Toff) operation.

Such a circuit exhibits a lower intrinsic limit for the controllable current. Indeed, the duty cycle of the wave at the output Q cannot decrease continuously to zero. Even if it were possible to control the duty cycle of this square wave to very low values, the bridge BR could not respond adequately to very short pulses. It follows that if it is desired to regulate the current in the load LD in an interval comprising both negative and positive values, the linearity of the regulation would be irreparably endangered around the null current values and in addition appropriate circuitry would be necessary to generate the signals L1 and L2.

The purpose of the present invention is to supply a method of driving by the PWM procedure for bridge circuits and a circuit operating consequently and which would permit overcoming the shortcomings of the prior art.

The purpose is achieved by means of the method

having the functions set forth in claim 1 and by means of the circuit having the characteristics set forth in claim 7. Additional advantageous aspects of the present invention are set forth in the dependent claims.

The present invention also relates to a disk drive in which the above mentioned method and circuit find advantageous application having the characteristics set forth in claim 15.

If instead of supplying to one of the two bridge circuit control inputs a conduction control signal having constant value and to the other a signal consisting of a virtually square wave two signals consisting of square waves are supplied to both the control inputs, the null current value will no longer constitute an intrinsic discontinuity and any value, even around zero, will be controllable with relative ease.

Then if it were desired to have variable regulation it would be particularly advantageous to set the duty cycle of both the square waves at 50% for the null current condition and vary the duty cycle of both the square waves in opposite directions and in accordance with the same law so as to obtain the best possible operating uniformity and symmetry.

The present invention is clarified by the description given below considered together with the annexed drawings in which:

FIG. 1 shows a known bridge circuit usable for the present invention,

FIG. 2 shows a known type of driving circuit,

FIG. 3 shows a driving circuit in accordance with the present invention in combination with a known type of bridge circuit,

FIGS. 4A,4B show two groups of time charts for voltage and current signals present in the driving circuit of FIG. 3 in two different operating conditions, and

FIG. 5 shows a block diagram of a disk drive in accordance with the present invention.

The method in accordance with the present invention is discussed with the aid of FIG. 1 which shows a bridge circuit of known type. On the market there are many other types of bridge circuit which can be used to implement the present invention. For example the integrated circuit L298N of SGS-THOMSON MICROELECTRONICS provides a double bridge circuit made up of bipolar transistors while the integrated circuits L6201, L6202 and L6203 of the above mentioned company provide bridge circuits made up of MOS transistors and also comprise a series of additional service circuits.

If to the two terminals C1 and C2 are sent two conduction control signals consisting of two virtually square waves, the transistors T1,T2 constituting a first half-bridge circuit and the transistors T3,T4 constituting a second half-bridge circuit are both started and stopped alternatively. By square wave is meant here merely a signal which can assume in a stable manner only two levels and is not necessarily periodic.

In the load LD current can run only if the transistors T1,T4 or T2,T3 are simultaneously in conduction. Hence, if the two square waves are virtually identical there will be virtually no current conduction in the load LD. If the two square waves are such that there are time intervals in which one of the two is at high level and the other at low level there is current conduction in the load during these difference intervals.

In reality the above statement is strictly true only for resistive loads. For inductive loads like direct current motors it is necessary to allow for the accumulated flow in the inductor. Specifically, during the difference intervals, to the load LD is applied the voltage present between the terminals I1 and I2 and hence the current in the load LD increases exponentially. During the rest of the time - the so-called 'recirculation' phase - the load LD is closed in a short circuit on itself and therefore the current in the load decreases exponentially. In general the time constants for charging and discharging are different and vary depending on operating conditions.

Regardless of the type of load, if the two square waves remain constant in frequency and phase long enough the average value of the current running in the load LD steadies at a rated operating value. This value depends on the duration of the difference intervals.

It is thus clear that there is no intrinsic limit on reduction of this duration because this limit is linked to the mutual position of the rising and falling edges of the two square waves.

If the two waves have the same frequency the average value of the current in the load depends on the value of the duty cycle. If the duty cycle is changed by at least one of the square waves, the average rated operating current changes.

If the duty cycle of both the square waves changes in the opposite direction the effect of changing the current is greater. And if the same change law is used for both, the effect will be double and in addition, if the duty cycle of both the square waves is set at 50% for the null current condition there is obtained the best possible operating uniformity and symmetry of the bridge circuit. For control purposes it is advantageous that the law be linear so as to have linear control.

If it is desired to provide current control of the feedback type at the output the duty cycle must be changed in relation to the average current supplied to the load and in particular if the load is inductive.

In the latter case the conduction control signals can be advantageously generated through the following steps.

a) Detection of the current supplied at the output 01-02,

b) generation of an error signal corresponding to

the average value of the difference between the detected current and a reference signal corresponding to the average current value desired at the output 01-02, and

c) generation of two difference signals of the logical type between the error signal and the two oscillating signals respectively in mutual phase opposition,

These two difference signals correspond to the conduction control signals, i.e. they can be used as they are or if necessary for example by adjusting the amplitude, level etc. thereof.

For methodological purposes it makes no different in step b) if the difference is found first and then the average value or vice versa.

The oscillating signals could be e.g. sinusoid or, to obtain linear control, triangular waves. For the present method it is not necessary that their frequency and amplitude of oscillation be constant in time provided they both change together, slowly and in the same manner.

This method is very simple and as a result can be provided in the circuitry as explained below.

A driving circuit providing the method in accordance with the present invention is shown in FIG. 3. This FIG. also shows a bridge circuit BR connected to the driving circuit and can be of known type like that shown in FIG. 1, of which the terminology will be used and to which will be coupled a load LD at the output 01-02 of the circuit BR.

The terminal I1 of the circuit BR is connected directly to the power reference VDD and the terminal I2 is connected directly to the ground reference GND.

The driving circuit comprises a first generator of virtually square waves and corresponds to a first comparator CO1 (FIG. 3) having its output coupled to the terminal C1 and a second generator of virtually square waves corresponding to a second comparator CO2 (FIG. 3) having its output coupled to the terminal C2. In this manner the conduction control signals of the bridge circuit BR consist of two square waves.

The comparator CO1 has a non-inverting input IP1 and an inverting input IN1. The comparator CO2 has a non-inverting input IP2 and an inverting input IN2.

In series with the load LD is located a resistor RS which acts as a detection circuit, in module and direction, of the current supplied at the output 01-02. There are other alternative ways of detecting, in module and direction, the current in the load of a bridge circuit. The resistor in series was chosen for its simplicity.

The voltage VS which develops across the resistor RS is sent to a differential amplifier consisting of an operational amplifier OA1 having an inverting input connected to one of the terminals of the resistor RS through a resistor R11, a non-inverting input connected to the other terminal of the resistor RS through a resistor R12 and a feedback output on the inverting input through a resistor R13 and in addition the non-inverting terminal is connected to a potential reference VM through a resistor R14. This potential is one half the potential of the power reference VDD.

To the driving circuit is also supplied a reference signal VI corresponding to the desired average value of the current at the output 01-02. The signal VI is sent to a differential amplifier consisting of an operational amplifier OA2 having an inverting input connected to a first terminal of a resistor R21, a non-inverting input connected to a first terminal of a resistor R22, and a fedback output on the inverting input through a resistor R23 and the voltage signal VI is applied to the second terminals of the resistors R21 and R22. In addition the non-inverting terminal is connected to the potential reference VM through a resistor R24.

The outputs of the operation amplifiers OA1 and OA2 are connected together respectively through a resistor RA and a resistor RB to the inverting input of an operational amplifier OA3. This amplifier exhibits a non-inverting input connected to the reference VM and is fedback by means of a feedback network connected between its output and its inverting input and consists of the parallel connection between a resistor RP and between a series connection of a resistor RZ and a capacitor CZ.

The entirety of the operational amplifiers 0A1, 0A2, 0A3 and of the dipoles connected thereto constitutes a comparator designed to generate an error signal VE corresponding to the average value of the difference between the current supplied and the current desired. This comparator has a low-pass transfer function mainly due to the pole introduced by the amplifier OA3.

The output of the amplifier OA3 is connected together with the inputs IP1 and IN2 respectively of the comparator CO1 and the comparator CO2. The inputs IN1 and IP2 receive respectively the two oscillating signals TR1 and TR2 in mutual phase opposition. Specifically they are triangular waves with virtually constant frequency having minimum value corresponding to the potential reference GND and maximum value corresponding to the potential reference VDD and hence average value equal to the value of the potential reference VM.

The voltage signals of the driving circuit exhibit a fixed and equal offset at VDD/2. This is linked to the fact that the bridge and the driving circuit are powered by means of the same positive-only potential power source. Nothing prevents having multiple power sources to avoid offset.

The circuit just described provides current control at the output of the feedback type. It is therefore essential to establish the regulation loop. For this purpose the feedback network of the amplifier OA3 introduces a zero to eliminate the effect of a pole usually introduced by the load of an electric motor.

If the average current supplied corresponds to the average current desired and is null, the voltage VE at the output of the amplifier OA3 is VDD/2. In this case the behavior of the signals TR1 and VE at the inputs of

the comparator CO1, of the signals TR2 and VE at the inputs of the comparator CO2, of the voltages at the terminals C1, O1, C2, O2 and of the current I-LD in the load is shown in FIG. 4A. It is noted that the duty cycle of both the square waves is 50%.

If the average current supplied corresponds to the average current desired and is positive, i.e. it comes out of the terminal O1, the voltage VE at the output of the amplifier OA3 is greater than VDD/2. In this case the behavior of the signals TR1 and VE at the inputs of the comparator CO1, of the signals TR2 and VE at the inputs of the comparator CO2, of the voltages at the terminals C1, O1, C2, O2 and of the current I-LD in the load is shown in FIG. 4B. It is noted that the duty cycle of the square wave at the terminals C1 and O1 is 50% greater than e.g., 15%, while the duty cycle of the square wave at the terminals C2 and O2 is 50% less than that amount, i.e. 15% in the example.

If the average current supplied corresponds to the average current desired and is negative, i.e. enters into the terminal O1, the voltage VE at the output of the amplifier OA3 is less than VDD/2 and the situation is the reverse of that of the last above case.

The linearity of the duty cycle variation is due to the decision to use triangular waves for the signals TR1 and TR2. The opposite direction of variation is due to the exchange of terminals of the comparators CO1 and CO2 and to the fact that the signals TR1 and TR2 are in mutual phase opposition. The offset of VDD/2 given by the reference VM involves the 50% duty cycle when the signal VI is null. To small positive or negative variations in this signal correspond small variations in the duty cycle of the two square waves and small variations in the load current with truly optimal linearity and low distortion.

It can be noted in particular from FIG. 4 that the wave frequency of the current I-LD is double the chopping frequency, i.e. of the switching frequency of the bridge circuit transistors. The result is that with respect to the circuits of the prior art the amplitude of the waves is less or that, for equal wave amplitude, a smaller chopping frequency can be chosen with resulting decrease in switching losses.

In the circuit of FIG. 3 the signals TR1 and TR2 were represented as though supplied at input to the driving circuit. It is possible to include in the driving circuit a circuitry designed to generate them. By selecting appropriately the topology of this circuitry it is possible that with a single triangular-wave generator and a small additional circuitry there can be achieved both of the signals and this has the advantage that the frequencies and phases of the two signals are rigorously coupled.

A driving circuit like that described lends itself to being integrated in a chip.

In such a chip, if necessary or desired, it is possible to integrate e.g. the bridge circuit and/or additional circuitry for auxiliary functions and/or even the entire control circuitry of a direct current electric motor as e.g. in the integrated circuit L6515 of SGS-THOMSON MICROELECTRONICS.

As already mentioned the driving circuit lends itself very well to use in a disk drive of which a very general block diagram is shown in FIG. 5.

This comprises a head H, an electromagnetic actuator VCM, typically a voice coil motor, for positioning of the head H, a motor SM for rotation of a disk DSK, a reading and/or writing control system RWCS connected to the head H, a position control system PCS connected to the actuator VCM and a rotation control system RCS connected to the motor SM.

More often, these disk drives comprise a certain number of disks and consequently a certain number of heads interconnected mechanically.

Disk drives of this type are used normally in personal computers both for floppy disks and hard disks. They generally require a card to be connected to the computer bus. Between the drive, in particular the RCS, PCS,RWCS control systems contained therein, and the card there is a continuous exchange of electrical signals CNTR including data to be written, data read, positioning commands, motor start and stop commands, etc..

The driving circuit in accordance with the present invention finds application in combination with a bridge circuit in the head position control system PCS. The actuator VCM is actually a translating motor in which movement depends on the average current circulating therein. By controling this current through the present driving circuit, which has good linearity, it is possible to achieve positioning of good accuracy.

For the motor SM it is generally preferred to use a brushless direct current motor with at least three windings requiring a different method and driving circuit. But if a common direct current spindle motor is used the driving circuit in accordance with the present invention could find application even in the rotation control system RCS.

Claims

1. Method of driving by the Pulse Width Modulation (PWM) procedure a bridge circuit (BR) of the type having a signal input (I1,I2) and a signal output (O1,O2) and at least two control inputs (C1,C2) receiving respectively at least two conduction control signals and in which one of said signals consists of a first virtually square wave and characterized in that the other of said signals consists of a second virtually square wave.

2. Method in accordance with claim 1 in which at least one of said waves has variable duty cycle.

3. Method in accordance with claim 2 in which the duty cycle of said waves is varied in opposite direction and preferably in accordance with the same linear law.

4. Method in accordance with one of claims 2 or 3 in

which the non-conduction condition of the bridge circuit corresponds to the condition in which said waves have 50% duty cycle.

5. Method in accordance with one of claims 2 to 4 in which the duty cycle is varied in relation at least to the average current supplied by the bridge (BR) to said output (O1,O2).

6. Method in accordance with claim 5 in which said conduction control signals are generated through the steps of:

a) detection of the current supplied at the output (01-02),

b) generation of an error signal (VE) corresponding to the average value of the difference between the detected current (VS) and a reference signal (VI) corresponding to the average current value desired at the output (01-02), and

c) generation of two logical difference signals between the error signal (VE) and respectively two oscillating signals (TR1,TR2) in mutual phase opposition and in which these two difference signals correspond to said conduction control signals.

7. Circuit for driving by the PWM procedure a bridge circuit (BR) of the type having a signal input (I1,I2) and a signal output (O1,O2) and at least two conduction control inputs (C1,C2) and comprising a first virtually-square-wave generator (CO1) having its output coupled to one (C1) of said two control inputs and characterized in that it comprises a second virtually-square-wave generator (CO2) having its output coupled to the other (C2) of said two control inputs.

8. Circuit in accordance with claim 7 in which at least one of said generators (CO1,CO2) has an input (IP1,IN2) for control of the duty cycle of the generated wave.

9. Circuit in accordance with claim 8 in which the inputs (IP1,IN2) for control of the duty cycle of said generators (CO1,CO2) are coupled together and act on the respective generators (CO1,CO2) in such a manner that the duty cycle of the waves generated is varied in opposite direction and preferably in accordance with a linear law.

10. Circuit in accordance with claims 8 and 9 in which the non-conduction condition of the bridge circuit (BR) is obtained by generating waves with 50% duty cycle.

11. Circuit in accordance with claims 8 to 10 and comprising a feedback network having an input coupled to said signal output (O1,O2) to detect the average current supplied thereto and having an output coupled to the control inputs (IP1,IN2) of at least one of said generators.

12. Circuit in accordance with claim 11 and comprising:

a) a detection circuit (RS) for the current supplied to said signal output (O1,O2),

b) a first comparator (OA1,OA2,OA3) with a transfer function of low-pass type and having a first input coupled to the output of said detection circuit (RS) and a second input receiving a reference signal (VI) corresponding to the desired average value of the current at said signal output (O1,O2),

d) a second (CO1) and a third (CO2) comparators having two inputs (IP1,IN2) of mutually different type coupled together at the output of said first comparator (OA1,OA2,OA3) and two other inputs (IN1,IP2) of mutually different type receiving respectively two oscillating signals (TR1,TR2) in mutual phase opposition.

13. Circuit in accordance with claim 12 and comprising in addition at least one generator of virtually triangular waves and having at least one output coupled to said two other inputs (IN1,IP2).

14. Circuit in accordance with one of the above claims and realized in integrated form in a chip.

15. Disk drive comprising at least a head (H), an electromagnetic actuator (VCM) for positioning of said head (H), a motor (SM) for rotation of said disk, a reading and/or writing control system (RWCS) connected to said head (H), a position control system (PCS) connected to said actuator (VCM) and a rotation control system (RCS) connected to said motor (SM) and in which said position control system (PCS) comprises a bridge circuit and a driving circuit in accordance with one of the above claims.

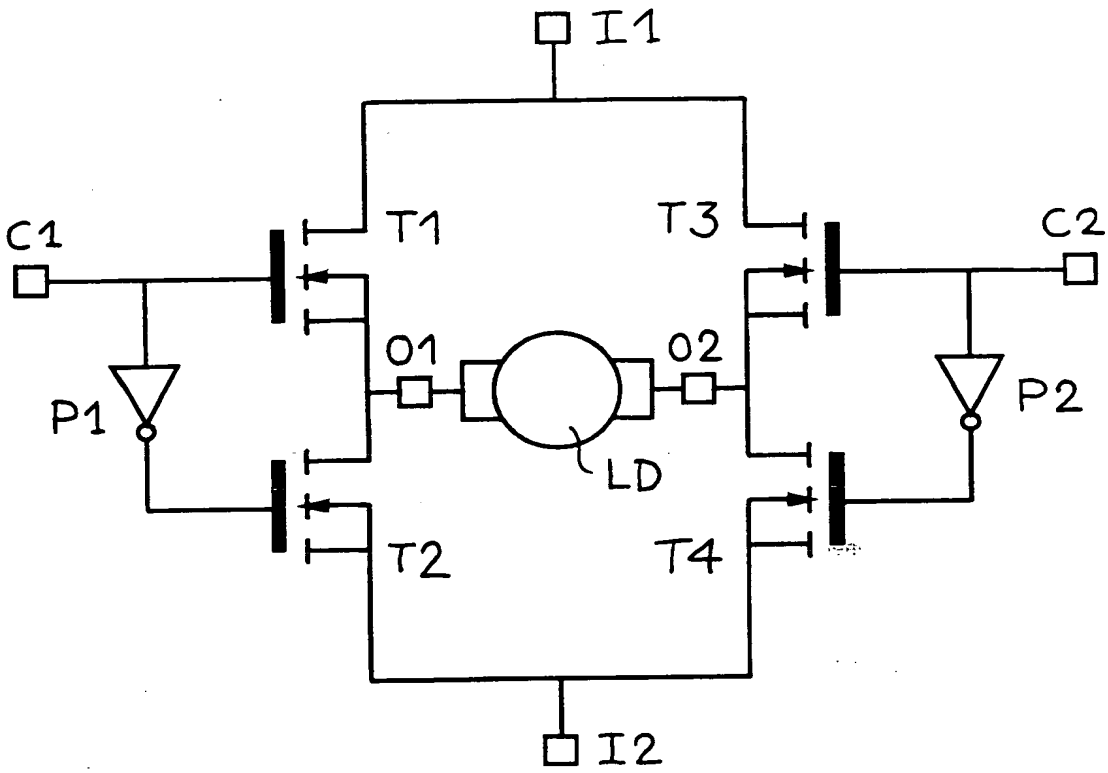
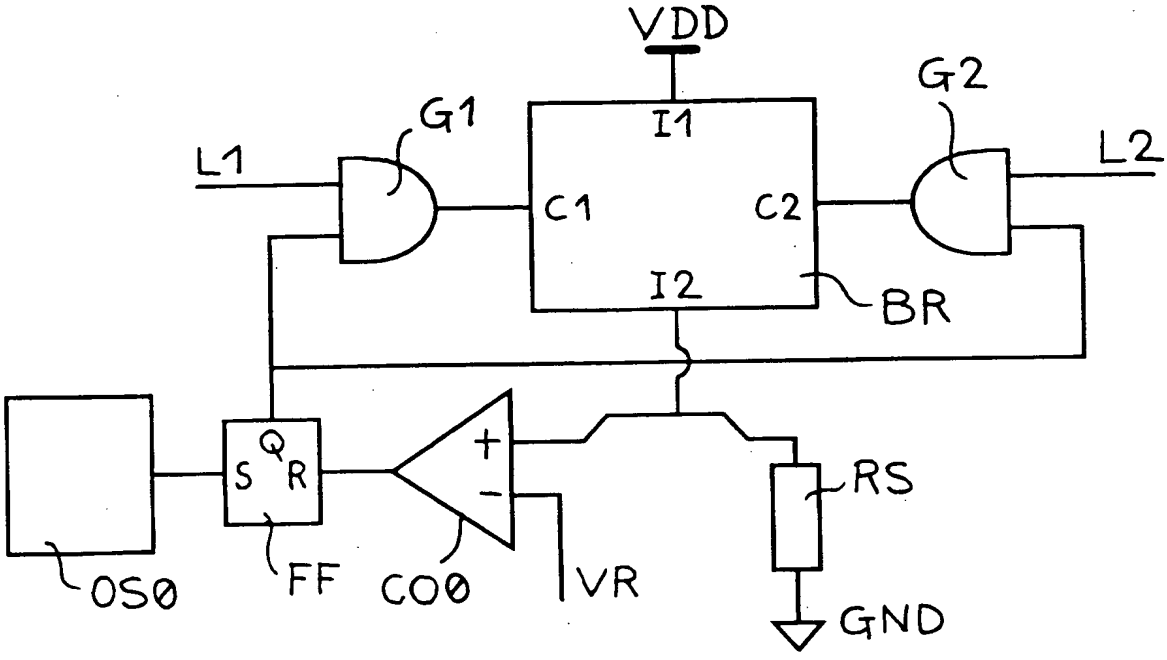

I1
C1
T1
T3
C2
O1
O2
P1
P2
LD
T2
T4
I2

Fig.1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G1
I1
G2
L1
L2
C1
C2
I2
BR
S
Q
R
RS
OS0
FF
CO0
VR
GND

Fig.2

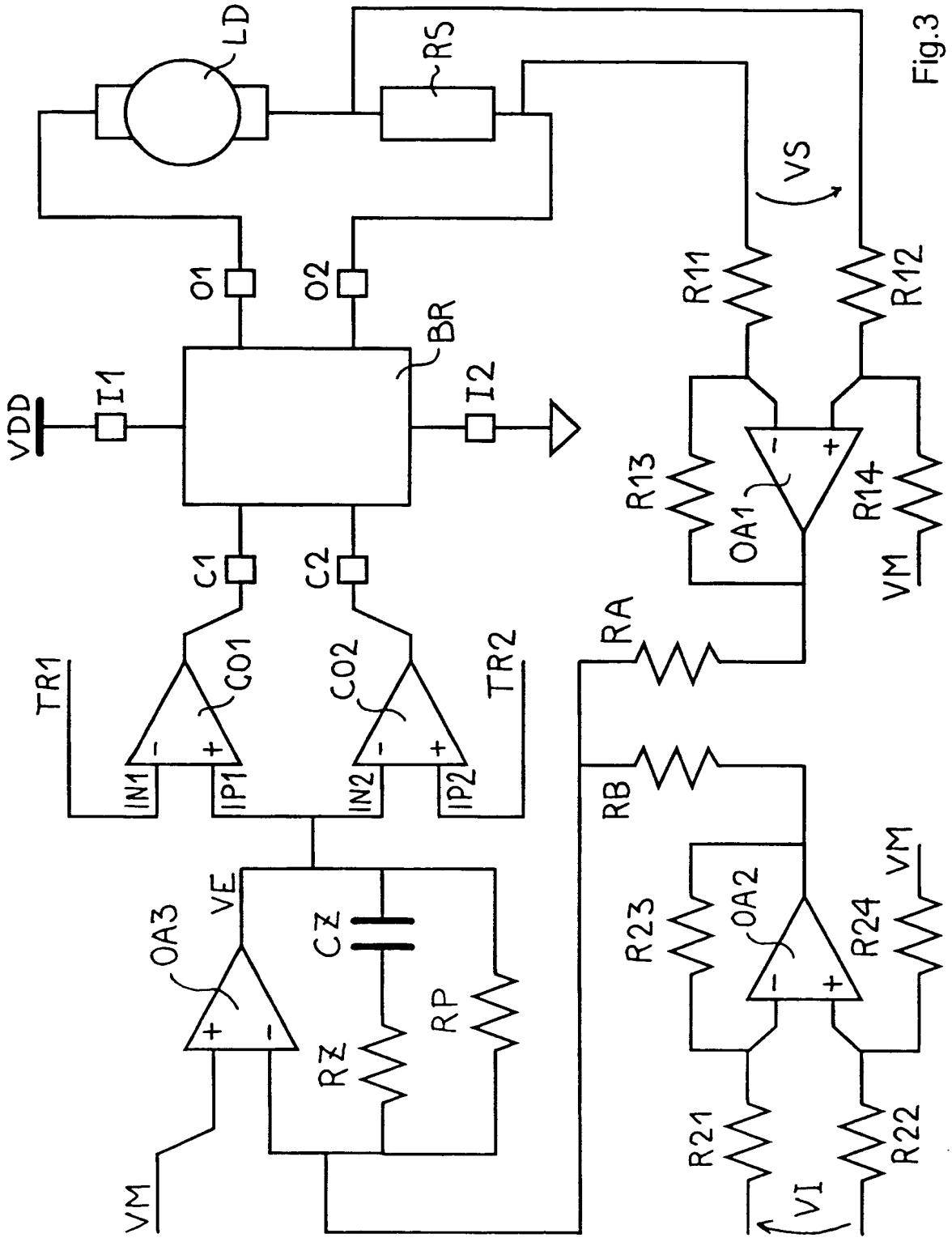

Fig.3

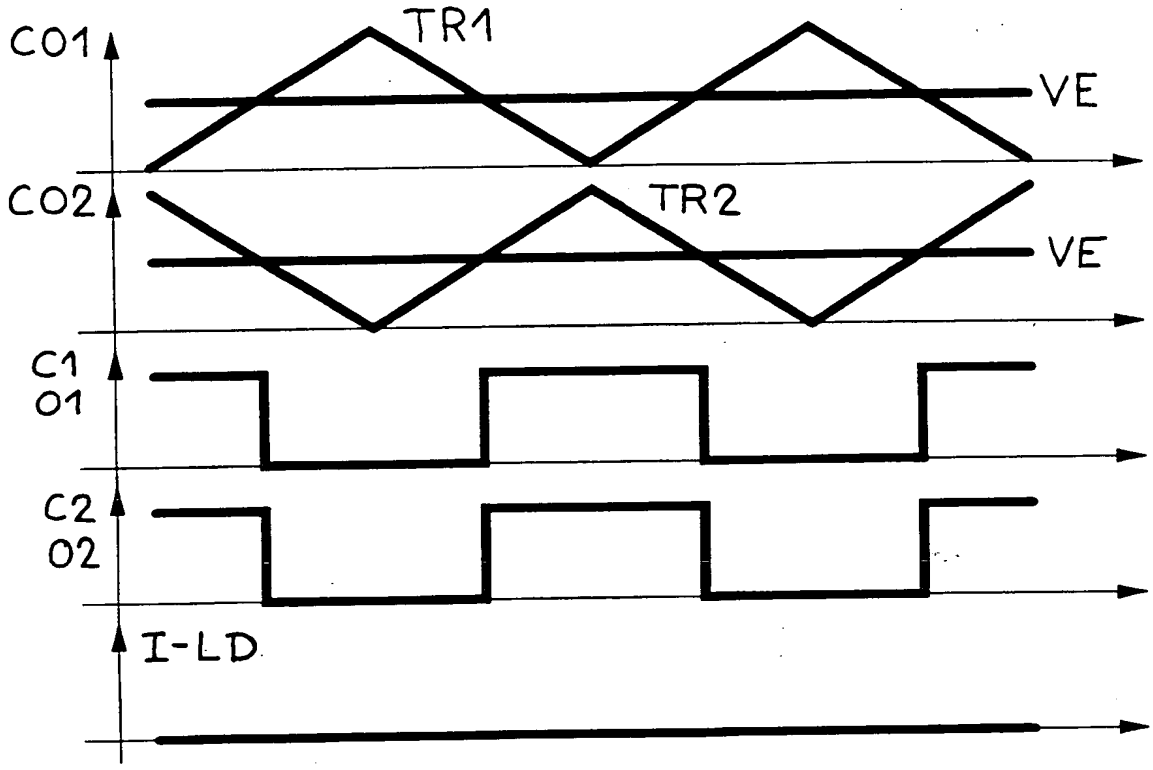

Fig.4A

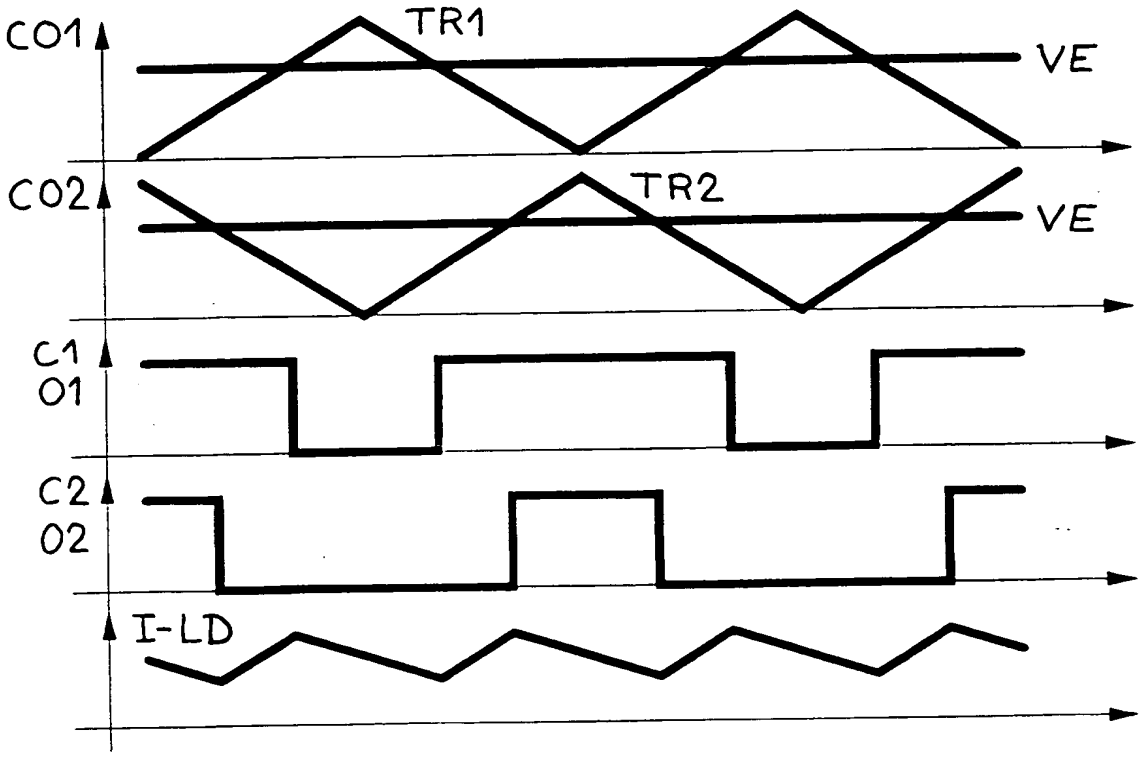

Fig.4B

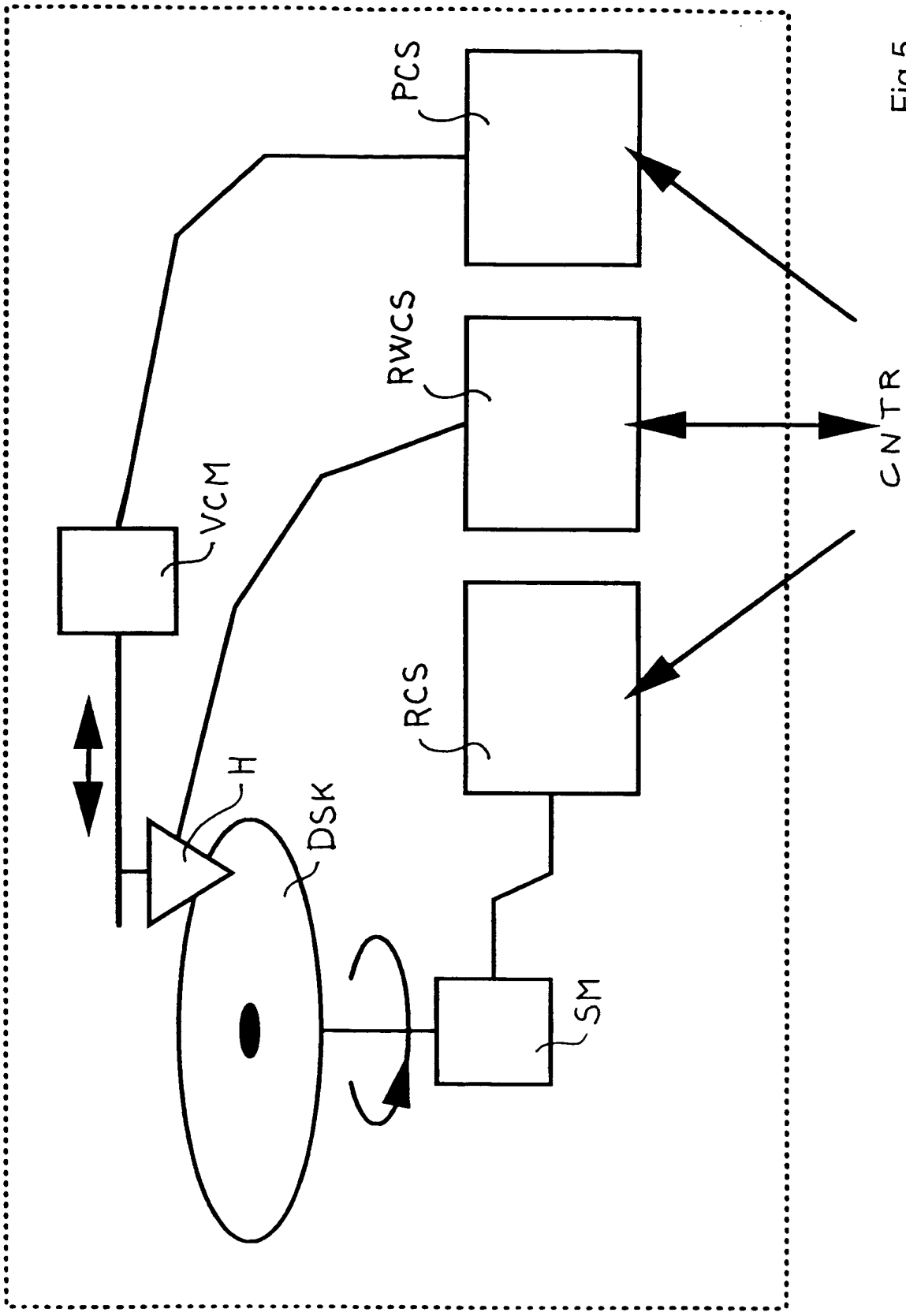

Fig.5

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 95 83 0371

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X Y	EP-A-0 441 459 (PIONEER ELECTRONIC CORP) 14 August 1991 * page 9, line 6 - page 10, line 14; figures 6-8 *	1-4, 7-10,15 5,6, 11-14	H02M7/5387 H02P7/00
Y	US-A-5 153 492 (LANDSEADEL BRADLEY A) 6 October 1992 * the whole document *	5,6, 11-14	
X	US-A-5 365 422 (CLOSE ERIC C ET AL) 15 November 1994 * column 4, line 29 - column 6, line 43; figures 1,2 *	1-4,7-11	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

H02M
H02P

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	29 January 1996	Gentili, L

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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